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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/921,423	08/02/2001	Randhir P.S. Thakur	3978.1US (95-0064.1)	8029

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EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/12/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/921,423	THAKUR ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *11* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/24/2002 has been entered.

Information Disclosure Statement

The examiner has considered the items listed in the Supplemental Information Disclosure Statement filed 10/15/2002 and entered as Paper No. 11. It is pointed out that the examiner previously has made the Haller reference of record to Applicant, and in fact features in the art rejections of Papers 4 and 6.

Response to Arguments

2. Applicant's arguments filed 08/29/2002 and 09/24/2002 have been fully considered but they are not persuasive.

In particular, while the amended claim language presently calls for the semiconductor device of the invention to have "at least one memory cell having a capacitor cell formed of multiple layers of glass", the primary reference (Hsia et al. (5,827,783)) teaches a capacitor cell for a memory device (cf. column 2, line 60-63),

said capacitor cell inherently being the memory cell of the memory device, capacitance being the physical property exploited in retaining charges and thereby create memory. Clearly, both the invention of Applicant and the primary reference are concerned with corrugated capacitor cells in DRAM memory devices, to increase storage capacity, while said storage capacity has to be accomplished in memory cells.

Moreover, the further limitation that the capacitor cell be "formed of multiple layers of glass" is implicit in the old limitations, reciting either at least one layer of boro-phospho-silicate glass and at least one layer of germanium boro- phospho-silicate glass, or a plurality of layers of boro- phospho-silicate glass and a plurality of germanium boro- phospho-silicate glass. Finally, with regard to Remarks by Applicant previously filed 08/29/2002 concerning the traverse of the Final Rejection (Paper No. 6) the additional references for claim 1, i.e., Wolf and Haller only serve to teach the material selection of the first non-conductive oxide and second non-conductive oxide in the primary reference (Hsia et al, 5,827,783)). It is already clear from the primary reference that necessary and sufficient requirements for the two materials are (a) that they must be non-conductive oxides, (b) that they must have standard use as dielectric in capacitors and that they must have substantially different etch rates. Wolf recites the plurality of reasons for the selection of BPSG (a non-conductive oxide) as a preferred dielectric in capacitors as enumerated in the Final Rejection (ease of deposition at relatively low temperature, reduced stress, relatively low glass flow temperatures), while, as detailed in the Final Rejection, Haller specifically teaches (see inter alia Figures 2 and 3 giving the etch rate as a function of etch rate and germanium

concentration) the exploitation of the strong dependence on germanium concentration of the etch rate of germanium-BPSG in the field of semiconductor integrated circuits, particularly patterned layers or regions of conductive and non-conductive materials in semiconductor integrated circuits, of which storage capacitors form a good example; therefore, Haller makes it clear that BPSG and Ge-BPSG also satisfy the third criterion, and hence the preference of BPSG and Ge-BPSG is not at all adversely affected by said third criterion. In conclusion, the examiner has regretfully no choice but to maintain the art rejections.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claim 1*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Wolf et al (ISBN 0-9616721-6-1) and Haller et al (5,804,506). With reference to Figs. 6-8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, comprising:

at least one layer of a nonconductive oxide with a first etch rate 62 (cf. column 5, lines 33-35);

at least one layer of a nonconductive oxide with a second etch rate 64 (cf. column 4, line 66 – column 5, line 1);

said nonconductive oxide layer with second etching rate having a portion contacting at least a portion of said at least one layer of nonconductive oxide with first etching rate.

Hsia et al do not necessarily teach the nonconductive oxide with first etch rate to be boro-phospho silicate glass and the nonconductive oxide with second etch rate to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the dielectric in capacitors in the semiconductor device art as evidenced by Wolf et al because of ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures (pages 198-201), while it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 – P_2O_5 – S_iO_2$, hence a nonconductive oxide) for the aforementioned at least one layer 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned at least one layer 64.

3. ***Claim 2*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Wolf et al (ISBN 0-9616721-6-1) and Haller et al (5,804,506). With reference to Figs. 6-8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, comprising:

a plurality of layers of a nonconductive oxide with a first etch rate 62 (cf. column 5, lines 33-35);

a plurality of layers of a nonconductive oxide with a second etch rate 64 (cf. column 4, line 66 – column 5, line 1);

at least a portion of at least one layer of said plurality of nonconductive oxide layers with second etching rate contacting at least a portion of at least one layer of said plurality of nonconductive oxide with first etching rate (cf. Figs. 6-8).

Hsia et al do not necessarily teach the nonconductive oxide with first etch rate to be boro-phospho silicate glass and the nonconductive oxide with second etch rate to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the dielectric in capacitors in the semiconductor device art as evidenced by Wolf et al because of ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures (pages 198-201), while it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate

glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 - P_2O_5 - S_iO_2$, hence a nonconductive oxide) for the aforementioned at nonconductive oxide 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive 64.

4. ***Claim 3*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Wolf et al (ISBN 0-9616721-6-1) and Haller et al (5,804,506). With reference to Figs. 6-8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, comprising:

a plurality of layers of a nonconductive oxide (with a first etch rate) 62 (cf. column 5, lines 33-35);

a plurality of layers of a nonconductive oxide (with a second etch rate) 64 (cf. column 4, line 66 – column 5, line 1);

each layer of said plurality of layers 64 having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers 62 (cf. Figs. 6-8).

Hsia et al do not necessarily teach the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a

standard choice for the dielectric in capacitors in the semiconductor device art as evidenced by Wolf et al because of ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures (pages 198-201), while it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 - P_2O_5 - S_iO_2$, hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

5. ***Claim 4*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Wolf et al (ISBN 0-9616721-6-1) and Haller et al (5,804,506). With reference to Figs. 6-8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, comprising:

at least one layer of a nonconductive oxide (with a first etch rate) 62 (cf. column 5, lines 33-35);

at least one layer of a nonconductive oxide (with a second etch rate) 64 (cf. column 4, line 66 – column 5, line 1) having at least a portion thereof contacting at least a portion of said at least one layer 62 (cf. Figs. 6-8).

Hsia et al do not necessarily teach the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the dielectric in capacitors in the semiconductor device art as evidenced by Wolf et al because of ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures (pages 198-201), while it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 – P_2O_5 – S_iO_2$, hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

6. ***Claim 5*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Wolf et al (ISBN 0-9616721-6-1) and Haller et al (5,804,506). With reference to Figs. 6-8: Hsia et al teach a semiconductor memory device (cf.

column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, comprising:

a plurality of layers of a nonconductive oxide (with a first etch rate) 62 (cf. column 5, lines 33-35);

a plurality of layers of a nonconductive oxide (with a second etch rate) 64 (cf. column 4, line 66 – column 5, line 1) at least a portion of at least one layer of said plurality of layers 64 contacting at least a portion of at least one layer of said plurality of layers 62 (cf. Figs. 6-8).

Hsia et al do not necessarily teach the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the dielectric in capacitors in the semiconductor device art as evidenced by Wolf et al because of ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures (pages 198-201), while it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 – P_2O_5 – S_iO_2$, hence a nonconductive oxide) for the aforementioned at

nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

7. ***Claim 6*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Wolf et al (ISBN 0-9616721-6-1) and Haller et al (5,804,506). With reference to Figs. 6-8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, comprising:

a plurality of layers of a nonconductive oxide (with a first etch rate) 62 (cf. column 5, lines 33-35);

a plurality of layers of a nonconductive oxide (with a second etch rate) 64 (cf. column 4, line 66 – column 5, line 1), each layer of said plurality of layers 64 having at least a portion thereof contacting at least a portion of at least one layer of said plurality of layers 62 (cf. Figs. 6-8).

Hsia et al do not necessarily teach the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the dielectric in capacitors in the semiconductor device art as evidenced by Wolf et al because of ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures (pages 198-201), while it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed

by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 - P_2O_5 - S_iO_2$, hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

8. ***Claim 7*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Wolf et al (ISBN 0-9616721-6-1) and Haller et al (5,804,506). With reference to Figs. 7 and 8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, comprising: at least one capacitor cell 78 (cf. column 6, line 47) having a portion thereof formed by at least one layer of nonconductive oxide 62 (cf. column 5, lines 33-35) and at least one layer of non-conductive oxide 64 (cf. column 4, line 66 – column 5, line 1) having at least a portion thereof contacting at least a portion of said at least one layer of nonconductive oxide 62.

Hsia et al do not necessarily teach the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the dielectric in capacitors in the semiconductor device art as

evidenced by Wolf et al because of ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures (pages 198-201), while it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 - P_2O_5 - S_iO_2$, hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

9. ***Claim 8*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Wolf et al (ISBN 0-9616721-6-1) and Haller et al (5,804,506). With reference to Figs. 7 and 8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, comprising: at least one capacitor cell 78 (cf. column 6, line 47) having a portion thereof formed by a plurality of layers of nonconductive oxide 62 (cf. column 5, lines 33-35) and a plurality of layers of non-conductive oxide 64 (cf. column 4, line 66 – column 5, line 1), at least a portion of at least one layer of said plurality of layers 64 contacting at least a portion of at least one layer of said plurality of layers of nonconductive oxide 62.

Hsia et al do not necessarily teach the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the dielectric in capacitors in the semiconductor device art as evidenced by Wolf et al because of ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures (pages 198-201), while it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 - P_2O_5 - S_iO_2$, hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

10. ***Claims 9, 10 and 13*** *are rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al (5,827,783) in view of Wolf et al (ISBN 0-9616721-6-1) and Haller et al (5,804,506). With reference to Figs. 7 and 8: Hsia et al teach a semiconductor memory device (cf. column 1, line 6 and column 4, lines 12-13) having at least one memory cell having a capacitor cell (cf. column 2, line 60-62) formed of multiple layers of glass, comprising: at least one capacitor cell 78 (cf. column 6, line 47) having a portion thereof

formed by a plurality of layers of nonconductive oxide 62 (cf. column 5, lines 33-35) and a plurality of layers of non-conductive oxide 64 (cf. column 4, line 66 – column 5, line 1), each layer of 64 having at least a portion thereof contacting at least a portion thereof contacting of at least one layer of said plurality of layers 64 contacting at least a portion of at least one layer of said plurality of layers 62.

Hsia et al do not necessarily teach the nonconductive oxide layers 62 to be boro-phospho silicate glass and the nonconductive oxide layers 64 to be germanium boro-phospho silicate glass. However, the use of boro-phospho silicate glass (BPSG) is a standard choice for the dielectric in capacitors in the semiconductor device art as evidenced by Wolf et al because of ease of deposition at relatively low temperature, reduced stress, and relatively low glass flow temperatures (pages 198-201), while it has been known for years that germanium doping of boro-phospho silicate glass markedly increases the etch rate (both wet and dry) of boro-phospho silicate glass, as witnessed by Haller (Abstract, fifth and sixth sentence; column 2, lines 65-67, and column 3, lines 17-24; cf. also Figs. 2 and 3).

Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Hsia et al at the time it was made so as to select boro-phospho silicate glass ($B_2O_3 – P_2O_5 – S_iO_2$, hence a nonconductive oxide) for the aforementioned at nonconductive oxide layers 62, and to select germanium boro-phospho silicate glass (also a nonconductive oxide) for the aforementioned nonconductive layers 64.

With regard to claim 10: the semiconductor memory device taught by Hsia et al further comprises at least one dielectric layer (cf. column 7, line 5) and a conductive

layer (cf. column 7, line 4) over said at least one dielectric layer ("over said" is not taught verbatim but examiner takes official notice that this is obvious in the art of capacitors generally and in the art of semiconductor memory device capacitors in particular, in the sense that otherwise one would not have a capacitor).

With regard to claim 13: the semiconductor memory device of Hsia et al further comprises at least one dielectric layer covering at least portions of said plurality of layers 62 and 64; and a conductive layer covering at least a portion of said dielectric layer (cf. column 7, lines 4-6).

11. ***Claim 11*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al, Wolf et al, and Haller et al as applied to claim 10 above, and further in view of Kawakubo (5,889,696). As detailed above, claim 10 (on which claim 11 depends) is unpatentable over Hsia et al in view of Wolf et al and Haller et al, neither of whom, however, specifically teach the semiconductor memory device of claim 10 with the further limitation as defined by claim 11.

However, particularly the use of BST as a high dielectric in capacitors in semiconductor memory devices has long been taught as a means to increase the charge storage capacity of capacitors, as witnessed, for example, by Kawakubo et al, who teach a semiconductor memory device (cf. Abstract, first sentence) with capacitor (cf. Abstract, first sentence) *for the very purpose of achieving very high charge storage* ability through the very high dielectric constant of BST (cf. column 9, lines 58-63). *Therefore, it would have been obvious* to one of ordinary skills in the art to modify the

invention by Hsia et al at the time it was made so as to include the further limitation of claim 11.

12. ***Claim 12*** *is rejected* under 35 U.S.C. 103(a) as being unpatentable over Hsia et al, Wolf et al, and Haller et al as applied to claim 10 above, and further in view of De Boer et al (5,930,106 and DERWENT copy, under "Novelty"). As detailed above, claim 10 (on which claim 12 depends) is unpatentable over Hsia et al in view of Wolf et al and Haller et al, who, however, do not specifically teach the conductive layer to comprise Si-Ge.

However, Si-Ge has long been taught as semiconductor memory device capacitor electrode material for the purpose of high reliability, as evidenced by De Boer et al, who teach a Si-Ge capacitor plate for the purpose of achieving high reliability (cf. particularly the DERWENT SUMMARY of De Boer et al) in a semiconductor memory device capacitor (cf. Abstract, final sentence; column 2, lines 24-28). Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention of Hsia et al at the time it was made so as to include the further limitation of claim 12.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
December 5, 2002

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